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India notifies Semicon 2.0 — Central Government support extended across semiconductor value chain

Executive summary

The Ministry of Electronics and Information Technology ('MeitY') has notified the Scheme for Development of Semiconductor Design and Manufacturing Ecosystem in India ('Semicon 2.0'/ 'the scheme'), the second phase of the India Semiconductor Mission ('ISM'), *vide* notification dated 31 August 2026.[1]

Semicon 2.0 covers six pillars and ten categories — semiconductor design, machines and materials, silicon, compound and display fabrication facility ('fabs'), ATMP / OSAT[2], advanced R&D and talent development. Fiscal support ranges from 25 per cent to 40 per cent of eligible capital expenditure for manufacturing categories, a deployment-linked incentive of 9 per cent of net sales for chip design, and up to 75 per cent of project cost for R&D and talent projects. Applications are open for an initial period of three years through ISM, the nodal agency.

For the first time, dedicated support is available for semiconductor equipment, sub-assemblies and semiconductor-grade materials, with entry thresholds starting at INR 50 crore of capital investment. The scheme materially broadens the opportunity for domestic and global companies across materials, equipment, fabs, packaging, design and R&D.

[1] Notification F. No. W-38/6/2025-IPHW, published in the Gazette of India.

[2] ATMP - Assembly, Testing, Marking, and Packaging; OSAT - Outsourced Semiconductor Assembly and Test

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Background

The Semicon India Programme (2021), with an outlay of INR 76,000 crore, established ISM as the nodal agency for developing a semiconductor and display manufacturing ecosystem in India. Under the first phase, the Government has approved 12 semiconductor manufacturing projects across six States with cumulative committed investment of over INR 1.64 lakh crore, comprising a silicon fab, compound semiconductor fabs and nine ATMP / OSAT units. Three facilities have commenced commercial production. In addition, 24 chip design projects have been approved and 105 start-ups / MSMEs supported under the Design Linked Incentive scheme.

The Union Cabinet approved the second phase of ISM in July 2026 and - MeitY notified the scheme for Semicon 2.0 in August 2026.

Key features of the scheme

- **Objective:** to build a self-reliant and globally competitive semiconductor design and manufacturing ecosystem, strengthen supply-chain resilience and establish technological leadership in critical sectors.
- **Coverage:** six pillars and ten categories — Design (C1 to C3), Machines and Materials (C4), Fabs (C5 to C7), Packaging (C8), R&D (C9) and Talent (C10).
- **Application window:** initially three years, through the ISM portal; mid-term appraisal of the scheme after three years of implementation.
- **Project duration:** preferably up to six years, decided on a project-by-project basis.
- **Appraisal and approval:** ISM evaluates applications on technical and financial parameters, including process technology, implementation capacity, operating capability and offtake arrangements, and forwards them to MeitY with its recommendation. Design and talent projects are approved by the Secretary, MeitY (project cost below INR 100 crore), the Minister (INR 100 crore to INR 500 crore) or the Union Cabinet (above INR 500 crore); all other categories are approved by the Union Cabinet.
- **Disbursement:** capex-linked fiscal support is disbursed on a pari-passu basis; revenue thresholds are tested in any of the three financial years preceding the year of application, including group companies and joint ventures.
- **Guidelines:** category-wise scheme guidelines, C-DAC Requests for Proposal for Category 1 and separate guidelines for Categories 9 and 10 are to be issued separately

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Fiscal support and thresholds

Category	Activity	Minimum investment	Revenue threshold	Fiscal support	Key condition
C1 Pillar 1	Strategic / national-importance design of IPs, chips, SoCs, modules	Not prescribed	Not prescribed	*To be specified through request for proposals ('RFPs') / detailed guidelines*	Indian-owned and controlled; C-DAC RFP and competitive bidding; IP co-owned with C-DAC
C2 Pillar 1	Commercial design of IPs, chips and SoCs (fabless)	Not prescribed	Not prescribed	DIS (EDA grid, MPW, IP cores, CSS, post-silicon validation); P-DLI — seed funding of 50% of project cost or Rs. 15 cr, lower (start-ups/MSMEs); equity co-investment; royalty financing	Indian citizen / OCI owned and controlled; IP and design files to remain in India
C3 Pillar 1	Deployment-linked incentive on newly launched IPs / chips / SoCs	Not prescribed	Not prescribed	9% of net sales for 5 years; cap Rs. 30 cr per application; Rs. 120 cr aggregate per company / group	First launch after scheme announcement, no prior sales; open to Cat. 1 and 2 applicants
C4 Pillar 2	Manufacturing ecosystem — (a) equipment R&D, (b) raw materials, (c) test & characterisation, (d) equipment mfg. / assembly	(a) Rs. 300 cr; (b) Rs. 50 cr; (c) Rs. 100 cr; (d) Rs. 300 cr	(a) Rs. 120 cr; (b) Rs. 20 cr; (c) Rs. 40 cr; (d) Rs. 120 cr	30% of capex, pari-passu. (d) additionally: PLI of 10% / 8% / 6% / 4% / 2% of domestically sourced BoM value for 5 years from FY 2028-29, capped at 50% of eligible capex	Own or possess licensed technologies (except test & characterisation)

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Category	Activity	Minimum investment	Revenue threshold	Fiscal support	Key condition
C5 Pillar 3	Silicon semiconductor wafer	Rs. 20,000 crore	Rs. 7,500 crore	40% of eligible capex, pari-passu	300 mm; 40,000 wafer starts / month or more; production-grade licensed technology
C6 Pillar 3	Compound semiconductors / photonics / sensors (incl. MEMS) / discrete fabs	Rs. 500 crore	Rs. 200 crore	35% of eligible capex, pari-passu	200 mm+ sensors; 150 mm+ compound & discrete; 100 mm+ photonics; 500 wafer starts / month or more
C7 Pillar 3	Display fabs — OLED, Micro LED and LCD	Rs. 10,000 cr (OLED); Rs. 1,500 cr (Micro LED); Rs. 10,000 cr (LCD)	Rs. 5,000 cr; Rs. 600 cr; Rs. 5,000 cr	35% of eligible capex, pari-passu	OLED Gen 6+ 30,000 panels/month; Micro LED 500 sq m/month; LCD Gen 8+ 60,000 panels/month
C8 Pillar 4	ATMP / OSAT — advanced and legacy packaging	Rs. 1,000 crore (both sub-categories)	Rs. 200 crore (both sub-categories)	Advanced packaging and advanced substrate: 35%; legacy packaging: 25% (of eligible capex, pari-passu)	Production-grade licensed technology for the proposed process
C9 Pillar 5	R&D for advanced semiconductor technologies	Not prescribed	Not prescribed	Up to 75% of project cost (capex + opex), including State incentive; may include part funding under the RDI Scheme	Separate detailed guidelines awaited; proposals considered by the Nodal Agency
C10 Pillar 6	Talent development across design and manufacturing	Not prescribed	Not prescribed	Up to 75% of project cost (capex + opex), including State incentive	Academic / R&D / scientific / domestic training institutions; separate guidelines awaited

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Implications for industry

Semicon 2.0 is the first Indian scheme to directly fund the upstream ecosystem — equipment, sub-assemblies and semiconductor-grade materials — alongside fabs, packaging, design, R&D and talent. The potential routes by investor segment are summarised below:[3]:

Investor segment	Potential Category	Key opportunity and consideration
Materials and chemicals	**C4**	Semiconductor-grade gases, chemicals, wafers, substrates and photoresists; 30% capex support with entry from INR 50 crore; anchor demand from fab and OSAT units under construction
Equipment manufacturers	**C4**	Manufacture / assembly of fab and packaging equipment and sub-assemblies; 30% capex support plus a BoM-linked PLI[4]; localisation near anchor customers
Fab / specialty semiconductor	**C5 / C6**	Silicon fabs at 40% and compound / photonics / sensor fabs at 35%; compound fabs accessible from INR 500 crore capex
Packaging / OSAT	**C8**	Advanced packaging and substrates at 35%; India's largest approved project cluster is ATMP / OSAT
Design / fabless and technology	**C1 / C2 / C3 / C9**	Design infrastructure access, seed funding, equity co-investment and a 9% deployment-linked incentive for Indian-incorporated, Indian-owned and controlled applicants; global players may participate through JV, consortium or licensing structures

[3] Potential applicability is subject to investment, technology, product and other scheme conditions. Operating in the semiconductor sector does not by itself confer eligibility.

[4] Bill of material/ Product-linked incentive

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Semicon 2.0 support may be combined with State Government incentives, subject to the respective State policy and its interaction with Central support. Gujarat, Uttar Pradesh, Odisha and Tamil Nadu have dedicated semiconductor policies, while Karnataka, Telangana, Andhra Pradesh, Maharashtra, Assam and Punjab treat semiconductor / ESDM as a thrust sector.

Support typically covers capital subsidy, land, power and electricity duty, stamp duty, employment / training and infrastructure. Location strategy can therefore materially influence the overall incentive package.

Our comments

- The scheme moves India's policy from supporting individual fabs to developing the complete value chain. Category 4 *(equipment and materials, with entry from INR 50 crore of capital investment)* opens the scheme to a much wider set of companies than the first phase; the 35 per cent versus 25 per cent differential in Category 8 is a clear signal in favour of advanced packaging.
- The application window is initially three years and the equipment PLI layer runs from FY 2028-29. Investors should map their India plans against category thresholds now, while category guidelines and RFPs are being finalised.
- Project structuring can significantly impact the overall incentive available. Key factors such as technology ownership/licensing, applicant or consortium structure, location in an SEZ versus Domestic Tariff Area ('DTA'), and the ability to combine Central and State incentives should be evaluated upfront. Accordingly, an eligibility assessment and incentive modelling should ideally be undertaken before finalising the investment location.
- Detailed guidelines and RFPs are awaited and may modify the operative position.



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